

ISL70444SEH SPICE Macro-Model

Introduction

The ISL70444SEH features four low-power amplifiers optimized to provide maximum dynamic range. These op amps feature a unique combination of rail-to-rail operation on the input and output as well as a slew enhanced front-end that provides ultra fast slew rates. They also offer low power, low offset voltage, and low temperature drift, making it ideal for applications requiring both high DC accuracy and AC performance. Manufactured in Intersil's PR40 SOI Process, the ISL70444SEH is immune to latch-up.

The SPICE model for the ISL70444SEH Rad Hard Quad Op Amp, was developed to help system designers evaluate the operation of this IC, prior or in conjunction with proto-typing a system design. This model accurately simulates typical performance characteristics at room temperature (+25 °C), such as frequency analysis, noise analysis, and slew rate analysis. Behaviors not supported are the bias current cancellation circuit and some temperature analysis. Functionality has been tested on ORCAD 10.0 and CADENCE ORCAD 16.5. Other SPICE simulators may be used, however, the model may require translation.

Reference Documents

- ISL70444SEH Data Sheet; [FN8411](#)
- ISL70444SEH SMD [5962-13214](#)

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Project Files

The zip file: **ISL70444SEH.zip** contains the project file modelcreator.opj to be used in ORCAD simulator. The project file has the model definition file (.lib), symbol file (.olb) and the schematic page as shown in Figure 1. The simulation profile is set up for AC analysis and sweeps parameter RF for various gain configurations. Figures 2 through 9 show a comparison of the simulation results versus bench results for various tests and it can be seen that the model approximates the IC very well.

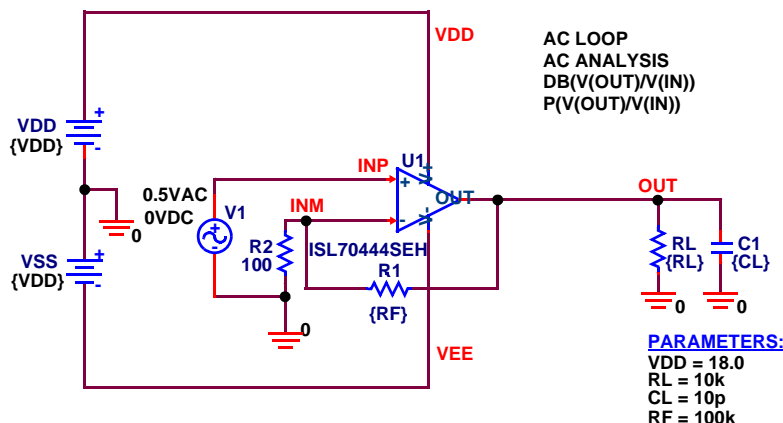


FIGURE 1. BASIC NON-INVERTING GAIN CONFIGURATION IN ORCAD SPICE FOR AC ANALYSIS

Simulation Performance Curves

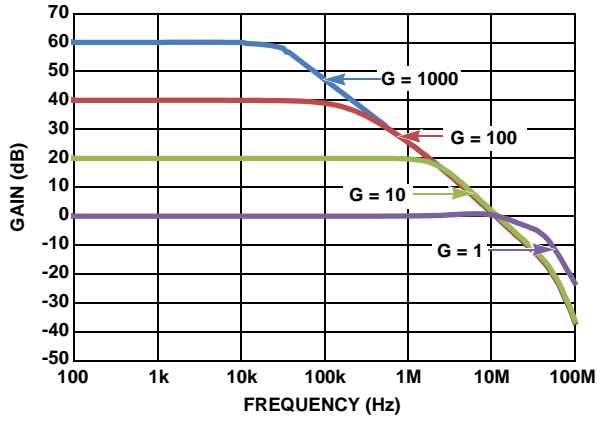


FIGURE 2. FREQUENCY RESPONSE vs GAIN, $V_S = \pm 18V$

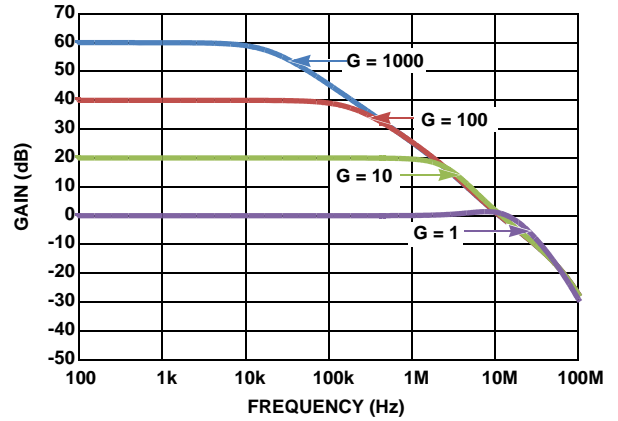


FIGURE 3. SIMULATED FREQUENCY RESPONSE vs GAIN, $V_S = \pm 18V$

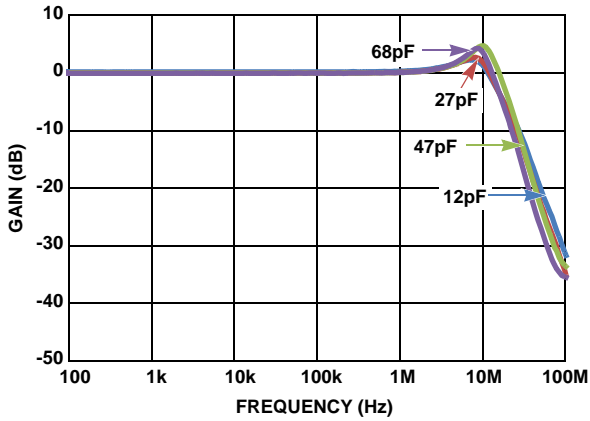


FIGURE 4. FREQUENCY RESPONSE vs CL

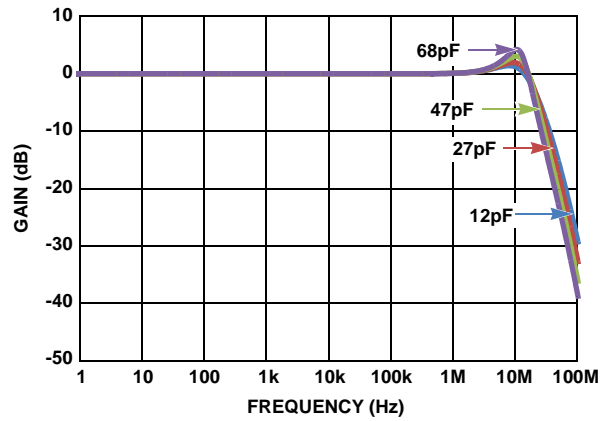


FIGURE 5. SIMULATED FREQUENCY RESPONSE vs CL

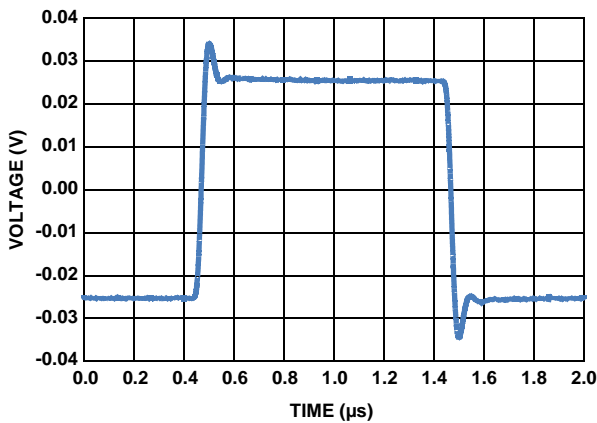


FIGURE 6. SMALL SIGNAL RESPONSE

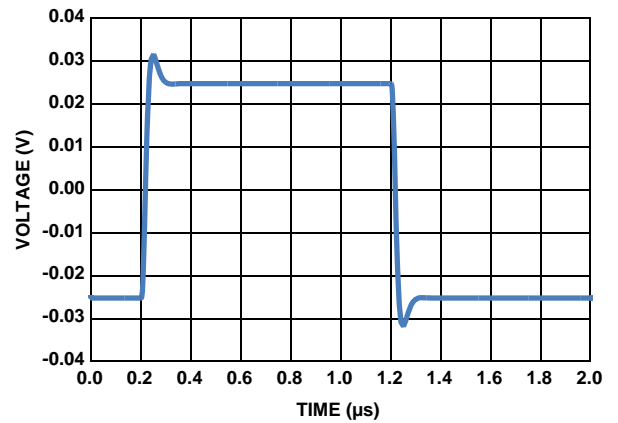


FIGURE 7. SIMULATED SMALL SIGNAL RESPONSE

Simulation Performance Curves (Continued)

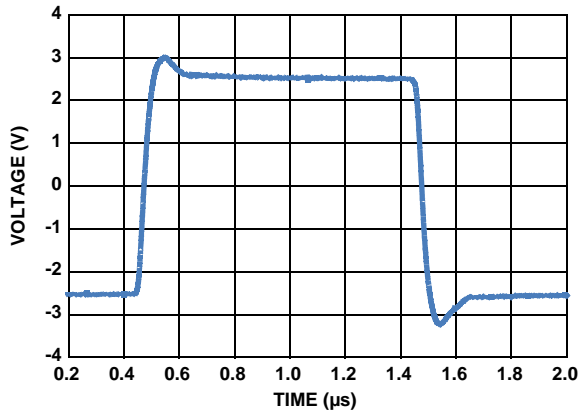


FIGURE 8. LARGE SIGNAL RESPONSE

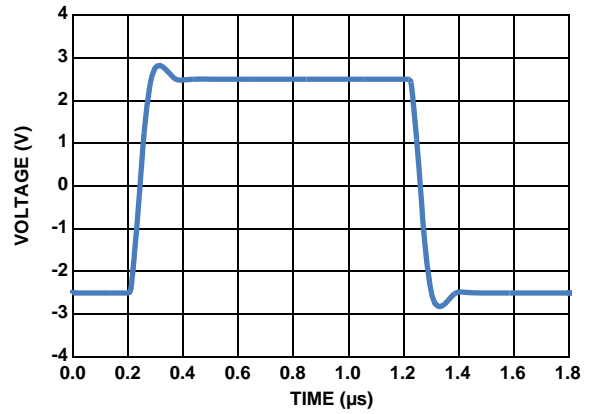


FIGURE 9. SIMULATED LARGE SIGNAL RESPONSE

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

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